HA-2542
SPICE OPERATIONAL AMPLIFIER MACRO-MODEL

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Introduction

This application note describes the SPICE macro-model for the HA-2542, a wideband, high output current, high slew rate op amp. The model was designed to be compatible with the well known SPICE program developed by the University of California in hope that most simulation software vendors follow this basic format and syntax. A schematic of the macro-model, the Spice net listing and various simulated performance curves are included. The macro-model schematic includes node numbers to help relate the SPICE listing to the schematic. The model is designed to emulate a typical rather than a worst case part. Most AC and DC paramaters are simulated. Significant poles and zeros are included to give the most accurate AC and transient simulation with minimum complexity.

Model Description

Input Stage

DP and DN represent the differential input resistance. Input bias currents are created by I1 and offset current is modeled with FA. Source VIO represents the input offset voltage. C1 limits slew rate. No input parasitics due to package capacitance and lead inductance are included.

Gain Stage

G2, R2, CC, GOL, and RD simulate open loop gain. CC is the macro-model dominant pole capacitor.

Poles and Zeros

The HA-2542 macro-model uses a complex pole and complex zero modeled with RLC networks as well as five poles and one zero.

General poles use RC networks and zeros use RL networks. Singularity frequencys are indicated on the schematic. Instructions for converting the model to have a simple two pole response are included in the netlist. This reduces simulation time at the expense of accurate frequency response.

Output Stage

EX1, D1 and D2 model output current limiting. IH and IL model the power supply currents. FIP and FIN vary the supply currents based on the op amps output current. DL, DH, VH and VL provide voltage clamping on the output to simulate the typical output voltage swing. No output parasitics due to package capacitance and lead inductance are included.

Parameters Not Modeled

To maintain a simple macro-model not all op amp parameters are modeled. Most of the parameters not modeled are listed below:

- Temperature Effects
- Differential Voltage Restrictions
- Input Voltage and Current Noise
- Common Mode Restrictions
- Tolerances for Monte Carlo Analysis
- Power Supply Range

Spice Listing

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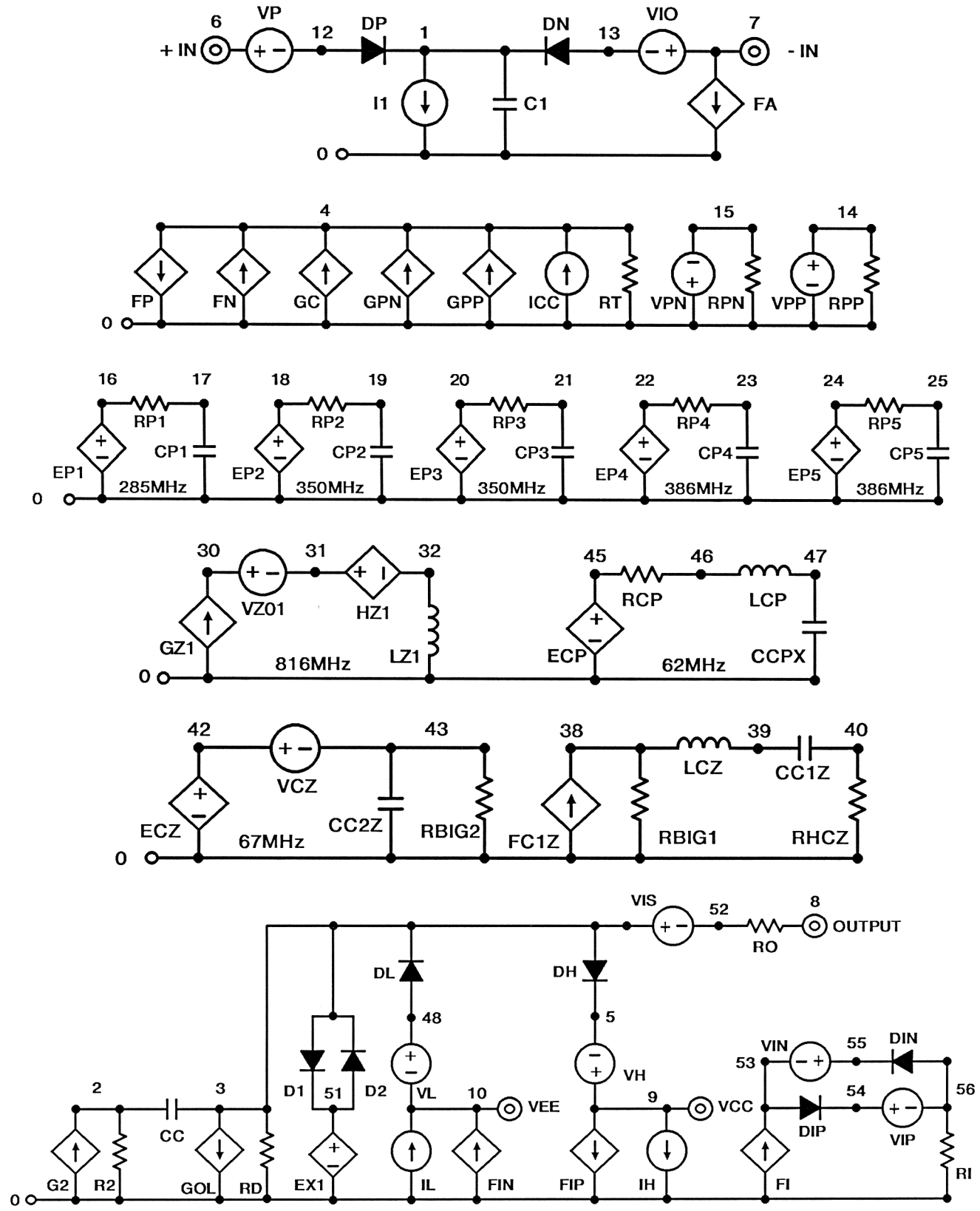
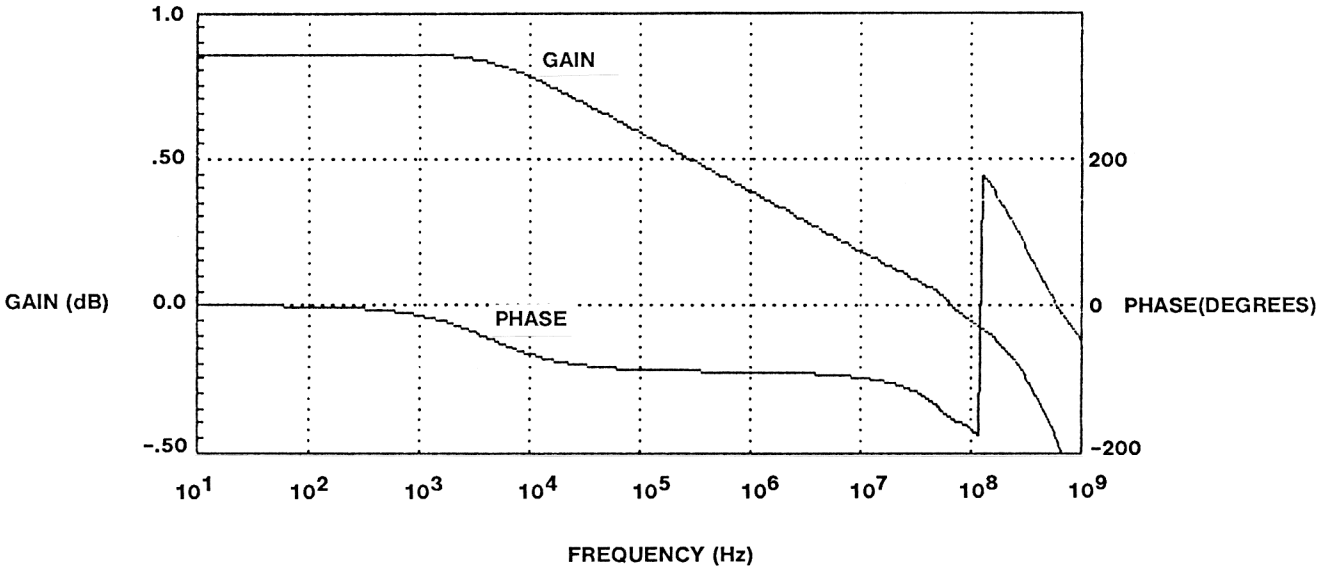
*
*HA-2542 MACRO-MODEL
*REV: 08-8-91
*BY: D.L. YOUNGBLOOD
*
*PINOUT CHANGED TO CONFORM TO "STANDARD"
*
*PINOUT:  +IN  -IN  VCC  VEE  VOUT
*
.SUBCKT  HA2542  6  7  9  10  8
.MODEL DP D      IS=1E-14          N=+2.1665E+01
.MODEL DN D      IS=+7.9827E-15    N=+2.1665E+01
.MODEL DV D      IS=1E-14          N=.1
.MODEL D1 D      IS=1E-14          N=1
.MODEL D2 D      IS=1E-14          N=+4.0513E-01
*
*INPUT STAGE
*
VP 6 12 0
DP 12 1 DP
*
*THE VALUE OF SOURCE "VIO" REPRESENTS OFFSET
*VOLTAGE AND MAY BE CHANGED TO SIMULATE
*WORST CASE, IF DESIRED
*
VIO 7 13 -1.4927E-03
*
DN 13 1 DN
FA 7 0 VIO +2.1680E-03
I1 1 0 +3.2477E-05
C1 1 0 +3.6662E-15  IC=-1.1864E+01
FP 4 0 VP  +4.2604E+02
FN 0 4 VIO  +5.3371E+02
GPP 0 4 9 14 +3.3536E-07
GPN 0 4 15 10 +1.0362E-06
RT 4 0 1.0
VPP 14 0 +1.5E+01
RPP 14 0 1K
VPN 0 15 +1.5E+01
RPN 0 15 1K
GC 0 4 1 0 +1.3823E-07
ICO 0 4 1.6400E-6
*
*GENERAL POLES
*
EP1 16 0 4 0 1.0
RP1 16 17 +5.5760
CP1 17 0 1.0E-10
EP2 18 0 17 0 1.0
RP2 18 19 +4.5425
CP2 19 0 1.0E-10
EP3 20 0 19 0 1.0
RP3 20 21 +4.5425
CP3 21 0 1.0E-10
EP4 22 0 21 0 1.0
RP4 22 23 +4.1259
CP4 23 0 1.0E-10
EP5 24 0 23 0 1.0
RP5 24 25 +4.1259
CP5 25 0 1.0E-10
*
*GENERAL ZEROS
*
GZ1 0 30 25 0 +1.9502E-04
VZ01 30 31 0.0
HZ1 31 32 VZ01    +5.1276E+03
LZ1 32 0 1.0E-6
*
*COMPLEX ZERO
*
ECZ 42 0 30 0 1.0
VCZ 42 43 0.0
CC2Z 43 0 +5.6373E-12
RBIG2 43 0 1.0E+7
FCZ 0 38 VCZ       1.0
LCZ 38 39 1E-6
CC1Z 39 40 +5.6373E-12
RHCZ 40 0 +2.2457E+02
RBIG1 38 0 1.0E+7
*
*COMPLEX POLE
*
ECP 45 0 38 0 1.0
RCP 45 46 +1.4226E+03
LCP 46 47 +6.5375E-06
CCPX 47 0 1.0E-12
*
*GAIN/OUTPUT STAGE
*
*FOR LEVEL 1 MODEL, CHANGE NODE 47 ON SOURCE "G2"
*TO 4, ADD A CAPACITOR FROM NODE 4 TO NODE 0 OF THE
*VALUE 3.282E-9, AND COMMENT OUT ALL POLES AND ZEROS
*
G2 0 2 47 0 1.0
*
R2 2 0 +2.3239E+05
CC 2 3 +2.2E-11
GOL 3 0 2 0 +7.3741
RD 3 0 +8.3965E-01
DH 3 5 DV
DL 48 3 DV
VH 9 5 4.2525
VL 48 10 2.6057
IH 9 0 +3.2170E-02
IL 0 10 +3.2206E-02
D1 3 51 D1
D2 51 3 D2
EX1 51 0 POLY  2  3  0  3  8  0  1  -6.3352E-01
RO 52 8 +3.37
VIS 3 52 0
FI 0 53 VIS  1
DIP 53 54 DV
DIN 56 55 DV
VIP 54 56 0
VIN 55 53 0
RI 56 0 1
FIP 9 0 VIP  1
FIN 0 10 VIN  1
.ENDS HA2542
```

Macro-Model Schematic

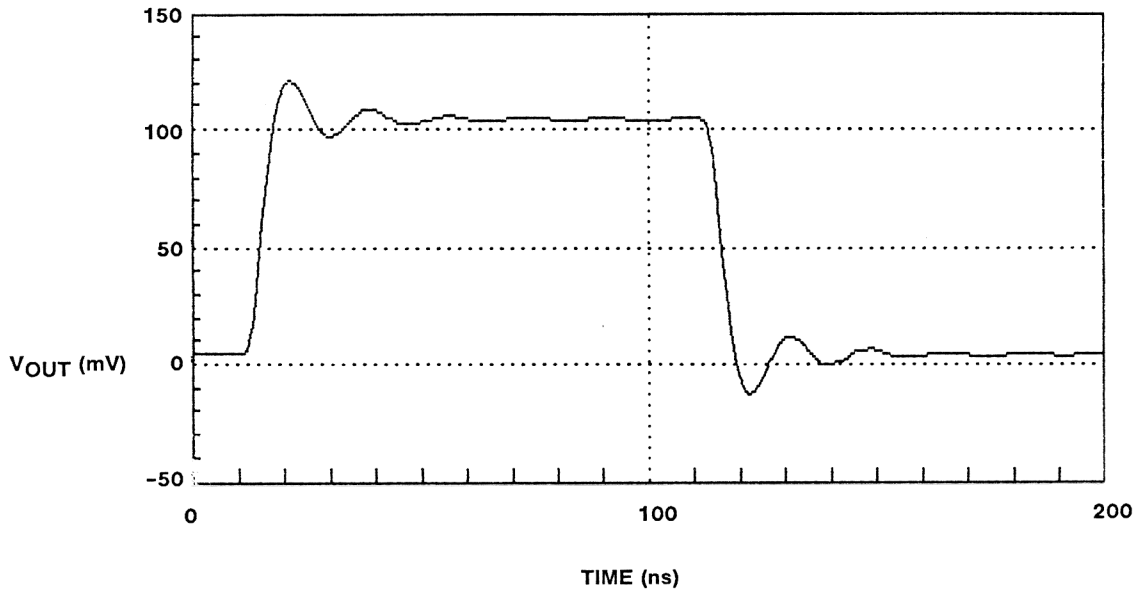


Model Performance Conditions V_{SUPPLY} = ±15 V, A_{VCL} = +2, Unless Otherwise Specified

OPEN LOOP GAIN AND PHASE vs FREQUENCY
(R_L = 1K, C_L = 10pF)

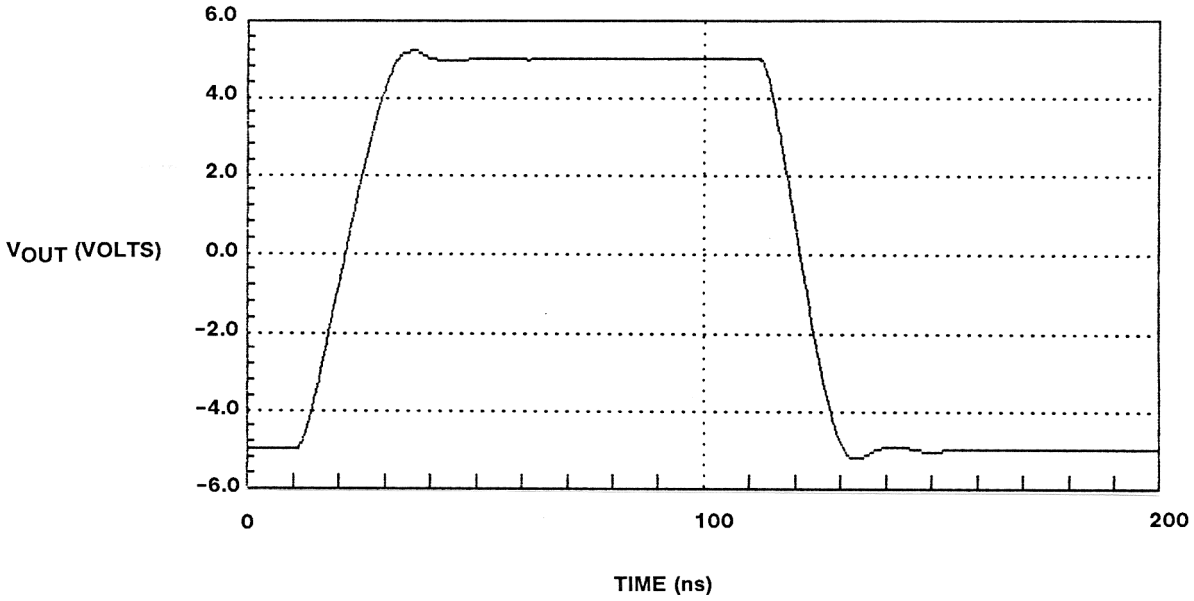


SMALL SIGNAL RESPONSE
(R_L = 1K, C_L = 10pF)



Model Performance **(Continued)** Conditions: V_{SUPPLY} = ±15V, A_{VCL} = +2, Unless Otherwise Specified

LARGE SIGNAL RESPONSE
(R_L = 1K, C_L = 10pF)



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